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Empirical Model for Drain Induced Barrier Lowering in Nano Scale MOSFET

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Abstract - The effect of variation of oxide design parameters on the Drain Induced Barrier Lowering in a conventional nano scale MOSFET has been studied, by theoretically proposing a new numerical method and verifying the empirical model by simulating with Sentaurus TCAD Toolkit. Since SiO_2 has its limitations at very low oxide thicknesses, improvement in the performance of the MOS by using high K dielectric material for Gate-channel isolation has also been studied. Empirical fitting parameters for accurately mapping the simulated data have been extracted.

Index Terms—Design parameters, Drain Induced Barrier Lowering, Simulation, Nanoscale, Sentaurus Toolkit, High-K dielectric, Empirical Modell

1 .INTRODUCTION:

The feature size of MOSFETs are being scaled down in order to keep pace with the miniaturisation standards [1], that has started with 10 µm half pitch of a standard memory cell in 1971, to have reached as low as 22nm in 2011 and is now all set to go down to 11nm in 2015 according to International Technology Roadmap for Semiconductors (ITRS) [2]. This has given rise to serious short channel effects [3], of which Drain Induced Barrier Lowering (DIBL) is a major limitation to the performance of the Nano scale MOSFETs [4 - 6]. Drain Induced Barrier Lowering is dependent on the values of the design parameters like substrate doping, oxide thickness, junction depth. etc. As the channel length scales down so does the oxide thickness. Beyond a minimum oxide thickness, the leakage current increases. If a high-K dielectric materials can replace SiO_2, this limitation is substantially reduced [7].

In this work, effect of scaling the dielectric material thickness on DIBL, has been studied. The effect of replacing SiO_2 by high-K material for gate isolation has also been investigated. A 45nm conventional enhancement n-MOSFET is studied analytically by computational theory [6, 8, 9] and its validity checked with results simulated by the powerful TCAD tool Sentaurus.

2.THEORY:

A short channel MOSFET with channel length less than the minimum value given by [10]

$$L_{min} = 0.4\{r_j t_{ox}(W_d + W_s)^2\}^5 \dots\dots\dots (1)$$

where r_j is the junction depth, t_{ox} is the oxide thickness and W_d and W_s are the depletion widths in the drain to substrate and source to substrate junctions respectively.

In case of short channel MOSFET, the threshold voltage (V_{th}) required to turn on the device is not constant. It changes with the variation of the drain to source voltage (V_{DS}). The variation in V_{th} is attributed to the lowering of the barrier between the source and the drain with the increase in V_{DS}. This change in threshold voltage is calculated as an index of DIBL. DIBL for bulk Si device is given by [6]

$$DIBL = 180\left(\frac{t_d t_{ox} V_{ds}}{S L_{eff}^2}\right)\dots\dots\dots\dots(2)$$

where S is the sub threshold swing, L_{eff} is the effective channel length and t_d is the depletion width given by

$$t_d \equiv \left(\frac{2\varepsilon_{Si}\psi_s}{qN_{Si}}\right)\dots\dots\dots\dots\dots\dots(3)$$

Subthreshold swing i.e.; change in subthreshold current due to small change in drain-source voltage is given by [6]

$$S = (60\text{mV})\left(1+\frac{t_{ox}\varepsilon_{Si}}{t_d\varepsilon_{ox}}\right)\dots\dots\dots(4)$$

It is evident from the above expressions that the DIBL parameter is dependent on the insulator thickness and the permittivity of the insulator.

For decades since the birth of MOSFET, SiO_2 has been the insulator of choice. However, with scaling, the SiO_2 layer faces the following challenges:

1. Direct tunnelling leakage current increases with the decrease in gate oxide thickness.
2. There is undesirable Boron diffusion from polysilicon gate through the oxide.
3. Reliability is poor.
4. Defect density increases.

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5. Uniformity of gate oxide is adversely affected.

A wider high-K dielectric insulating material may have the advantage of scaling minus the disadvantages inherent to scaled down SiO_2 layer.

The relationship between the oxide thickness and the DIBL parameter for submicron devices is first computed. It is then repeated for DIBL parameter variation for high K dielectric materials as alternative to SiO_2. Effect of high-K material on the effective thickness of the insulating layer that achieves the required isolation is measured by Equivalent Oxide Thickness (EOT) which is given by [7] as

$$EOT = t_{HK}\left(\frac{K_{SiO^2}}{K_{HK}}\right) \ldots\ldots\ldots (5)$$

Dielectric constants and band-gaps of high-k materials needed for computation are given in Table-I. [10]

TABLE – 1:

GATE MATERIAL	DIELECTRIC CONSTANT K	ENERGY BAND GAP (Eg)
SiO_2	3.9	9
TiO_2	80	3.5
HfO_2	25	6
Ta_2O_5	25	4.4
Al_2O_3	8	8.8
ZrO_2	25	5.8
$ZrSi_xO_y$	8-12	6.5
Y_2O_3	13	6
Ya_2O_3	27	4.3

Choice of gate oxide depends on permittivity K and energy band gap E_g. Table 1 indicates a few good quality dielectric materials. Here HfO_2 is the material of choice because of its high-K value and high band gap energy.

In this computation of DIBL parameter, the depletion width t_d in expression 2 is derived by solving two-dimensional (2D) Poisson's equation.

$$\frac{\delta^2 \Psi}{\delta x^2} + \frac{\delta^2 y}{\delta y^2} = \frac{-\rho}{\varepsilon} \ldots\ldots\ldots\ldots (6)$$

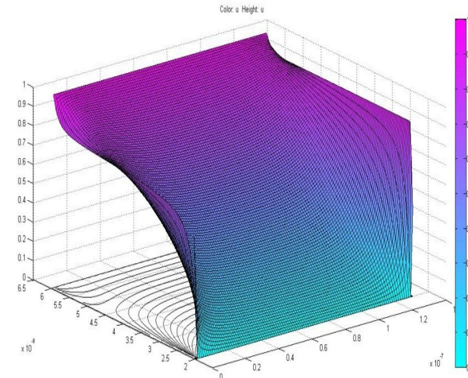
with total space charge density given by

$$\rho(x,y) = \{p(x,y) + N_d^+ - n(x,y) - N_a^-\} \ldots\ldots\ldots\ldots (7)$$

where n(x,y) and p(x,y) are electron and hole densities, N_a^- and N_d^+ are the ionised acceptors and donors respectively.
From equation 5 and 6 we have,

$$\frac{\delta^2 \psi(x,y)}{\delta x^2} + \frac{\delta^2 \psi(x,y)}{\delta y^2} = -\frac{2qN_i}{\varepsilon_s} \ldots\ldots (8)$$

Exact solution of Poisson's equation is analytically computed employing Finite Element Method (FEM) with the help of 'pde' toolbox from Matlab (Figure - 1). The Surface potential is calculated from this solution. Thus the depletion width t_d computed using the surface potential so obtained gives more exact result as compared to the assumed values of surface potential.



Figure–1: Potential Contour in Channel of N-MOSFET,Distance along X-axis represents channel width, Distance along Y-axis represents channel length, Distance along Z-axis represents channel potential

The analytical expression of DIBL is expected to provide better agreement with simulated results and as it is expected to yield more accurate value of the dielectric thickness t_d .

III. Results and discussions:

The simulation is done on the 45nm MOSFET shown in figure 2:

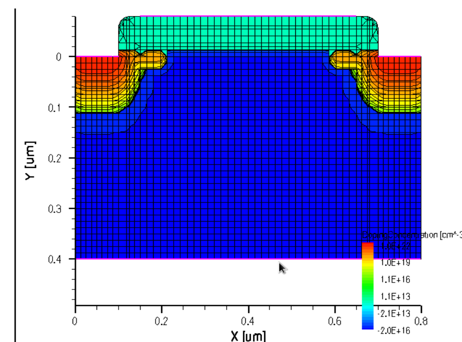


Figure – 2 : 45nm MOSFET after meshing, colour bar indicates the corresponding electron doping concentration

The effect of DIBl on drain current is shown in figure 3 where the drain field has ten folds increased the current current.

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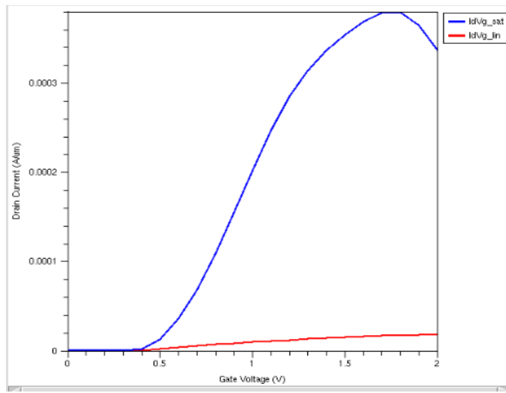


Figure –3: I_d-V_g Curve (saturation and linear):Gate Voltage along X-axis and Drain current along Y-axis

The effect of variation of design parameters on DIBL as obtained from simulated results are shown. TCAD SENTAURUS is used to simulate the n-MOSFET. Data is plotted in Matlab Software.

The results in figures 4 – 8 demonstrate the varitaion of DIBL parameter with the design partameters; substrate doping (Fig. 4), oxide thickness (Fig. 5), temperature (fig. 6), junction depth (Fig. 7) and drain-source voltage (Fig. 8).

Analytical results calculated from the expression given in reference [6] based on one-dimensional Poisson's equation, do not agree with well the simulated results. It is found that the deviation of calculated values diverge from the simulated ones. As the field in the channel increases the need for including the fringe effects and solving the two-dimensional potentials increase. By merely incorporating surface potential computed from solving the 2-D Poissons equation into the expression 2 [6] will not agree with the simulation unless the expression 2 is modified using the small channel effects. Hence we have opted for empirical modelling in order to obtain an accurate empirical model that will efficiently describe the DIBL effect to design engineers.

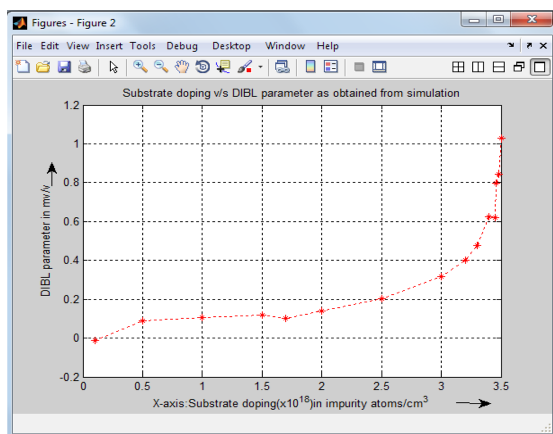


Figure – 4: DIBL vs Substrate doping:
DIBL along Y-axis, Substrate doping along X-axis

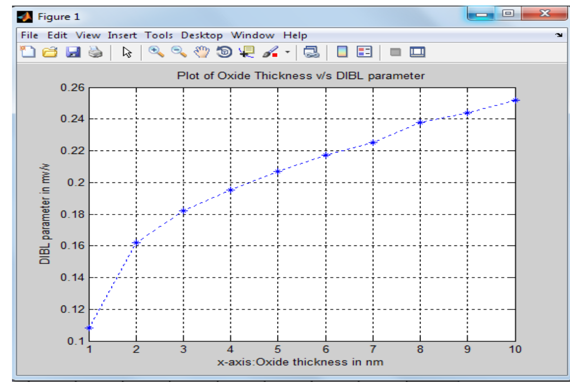
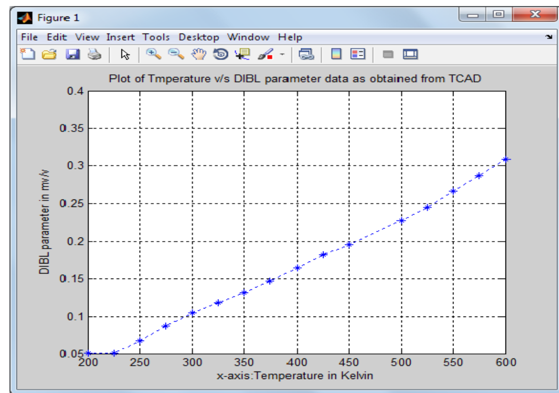


Figure – 5: DIBL vs Ox ide Thickness (in nm):
DIBL along Y-axis, t_{OX} (in nm) along X-axis



Figure–6: DIBL vs Temperature (in Kelvin):
DIBL along Y-axis, T (in Kelvin) along X-axis

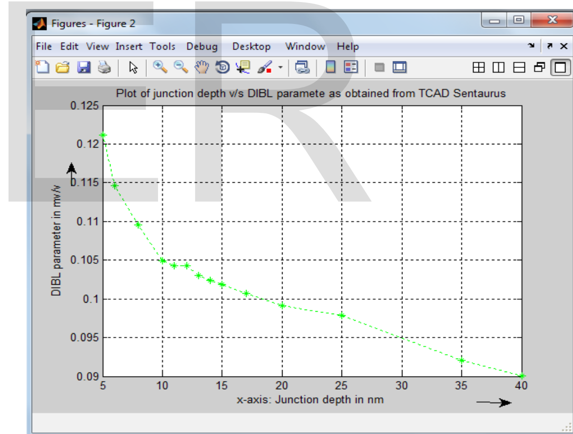


Figure – 7: DIBL vs Juntion dept(in nm):
DIBL along Y-axis, Juntion dept along X-axis

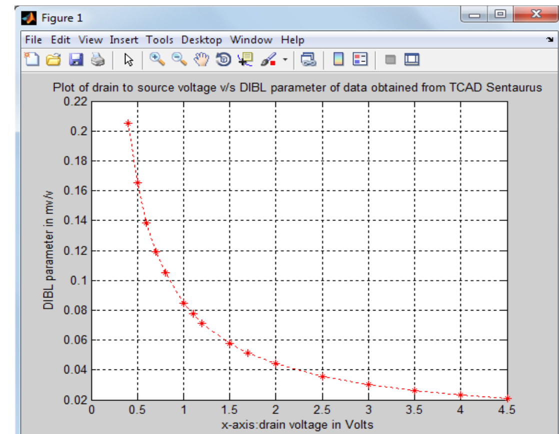


Figure 8 : DIBL vs drain-source voltage (in mV):
DIBL along Y-axis, V_{DS} along X-axis

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2.1 Proposed Model

There is a clear mismatch between the theoretical values of DIBL parameters and their simulated results. An empirical model is proposed for to correctly account for the effects of the design parameters. Empirical relations for the DIBL parameter for each individual design parameter, keeping others constant, are obtained by Polynomial Curve Fitting using Matlab® tool. It is assumed that individual effects of the design parameters are linearly separable.

2.2 Empirical relationship:

Drain to Source Voltage: Curve fitting of DIBL with V_{ds} can be with a 6th order polynomial. The curve is shown below (Fig 9). The empirical formula explaining the variation is

P_1 = [$0.0017x^0$ - $0.0269x^1$ + $0.1731x^2$ - $0.5689x^3$ + $1.0179x^4$ - $0.9763x^5$ + $0.4625x^6$]

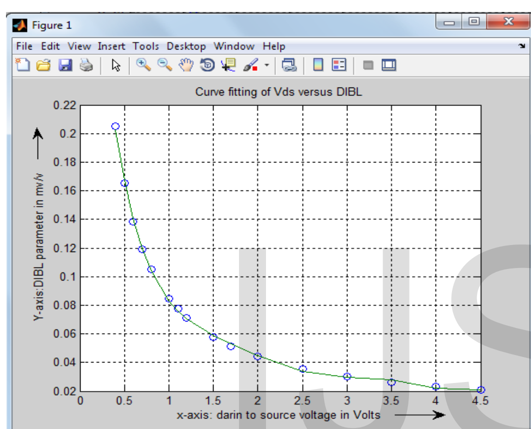

Figure -9: Curve fitting of DIBL with V_{ds}:
DIBL along Y-axis, V_{DS} (in mV) along X-axis

Junction Depth: Curve fitting of DIBL with junction depth (Fig 10) gives a 13th order polynomial with the following fitting curve

P_2=[$0.0x^0$ + $0.0x^1$ + $0.0x^2$ + $0.0x^3$ + $0.0x^4$ - $0.0012x^5$ + $0.0223x^6$ - $0.3127x^7$ + $3.2005x^8$ - $23.5756x^9$ + $121.4860x^{10}$ - $414.5655x^{11}$ + $839.2957x^{12}$ – $760.8183x^{13}$]

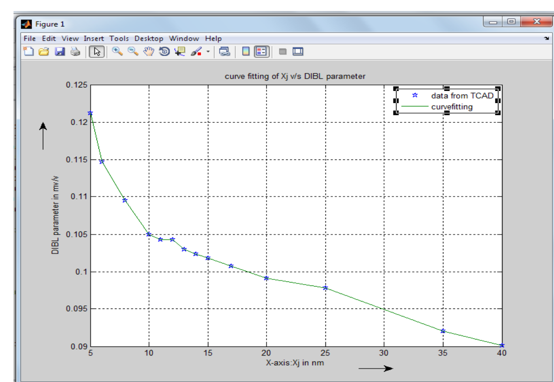

Figure-10: Curve fitting of DIBL with junction depth: DIBL along Y-axis, t_{OX} in nm) along X-axis

Temperature The Polynomial for fitting the variation of temperature with DIBL is a 1st order one. The relationship is P_3 = [$0.0007x^0$-$0.0927x^1$]

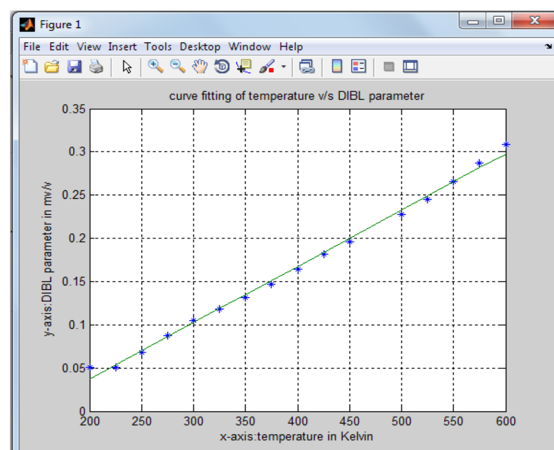

Figure-11: Curve fitting of DIBL with Temperature, DIBL along Y-axis, T(in Kelvin) along X-axis

Oxide thickness: The polynomial for curve fitting the variation of oxide thickness with DIBL is a 2nd order one. The curve fitting parameters are given in the row matrix P_4 = [$0.136x^0$ + $.128x^1$]

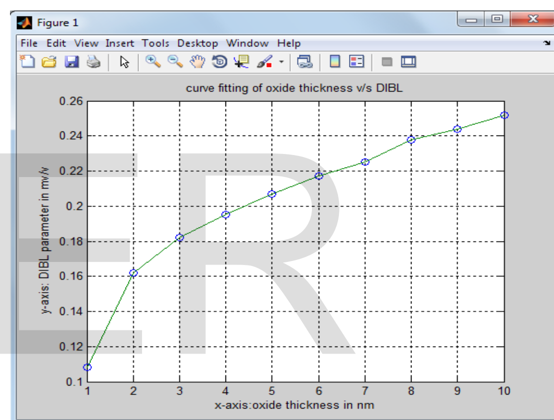

Figure-12: DIBL with Oxide Thickness(in nm): DIBL along Y-axis, t_{OX} (in nm) along X-axis

Substrate Doping: Variation of DIBL parameter with substrate doping is a 13th order polynomial:

P_5 = [$0.0001x^0$ – $0.0016x^1$+ $0.0126x^2$- $0.0658x^3$ + $0.239x^4$ - $0.6201x^5$+ $1.1554x^6$ -$1.5329x^7$ + $1.4120x^8$ - $0.8607x^9$ + $0.3179x^{10}$ - $0.0595x^{11}$ + $0.0035x^{12}$] .10^8

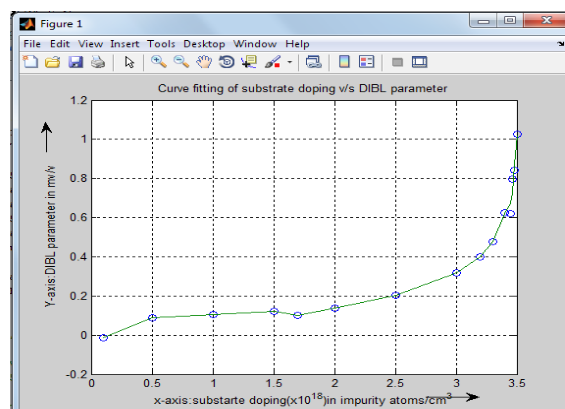

Figure-13: Curve fitting of DIBL with Substrate doping : DIBL along Y-axis, Substrate doping along X-axis

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Effect of High K-dielectric on DIBL:

In 45nm conventional n-MOSFET with oxide barrier, the effect of DIBL becomes significant. The effect of DIBL can be reduced if the silicon di-oxide is replaced by a high-K material with greater thickness. This thickness is refereed to as Effective Oxide Thickness (EOT). Fig. 14 plots the EOT (computed by equation 5) against permittivity for different high-K dielectrics. With the increase of permittivity for high-K dielectric, equivalent oxide thickness decreases. A wider high-K material can be used for channel isolation with the same effect as that of a much narrower oxide and hence the gate control over the channel remains unchanged but tunnel current is reduced. The effect of DIBL will decrease if a high-K material with lower EOT is used. Thus the choice of high-K dielectric improves the device behaviour at nano dimensions.

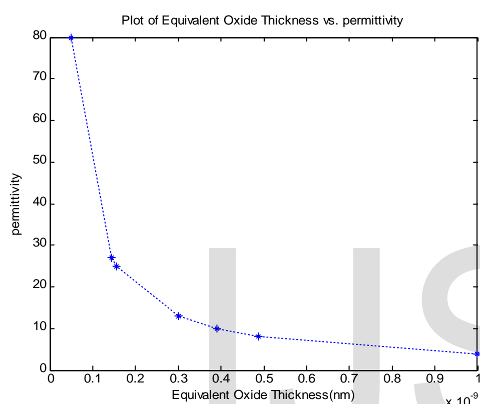

Fig. 14: Variation of EOT with permittivity

Effect of change of dielectric material is accounted for by the varying EOT. Effect of different insulating materials with different dielectric constants can be easily incorporated by computing the Effective Oxide Thicknesses. Alternatively, the EOT will help in calculating the thicknesses of the high-K materials needed for a particular DIBL parameter.

If a high-K dielectric layer is grown on substrate itself the interface becomes unstable due to mismatch in the lattice constant of the insulator and substrate. This causes increase in scattering and hence mobility degradation. Hence a solution is [7] to grow a low-K dielectric layer above the substrate and then grow the high-K layer. This will increase the EOT thus affecting the DIBL parameter.

IV. Conclusion:

It is therefore concluded that as the device is scaled down, DIBL becomes more and more pronounced. Hence gate geometry related solutions are sought for. But if the insulator thickness can be scaled down, the DIBL will be reduced which is definitely a positive effect of scaling.

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